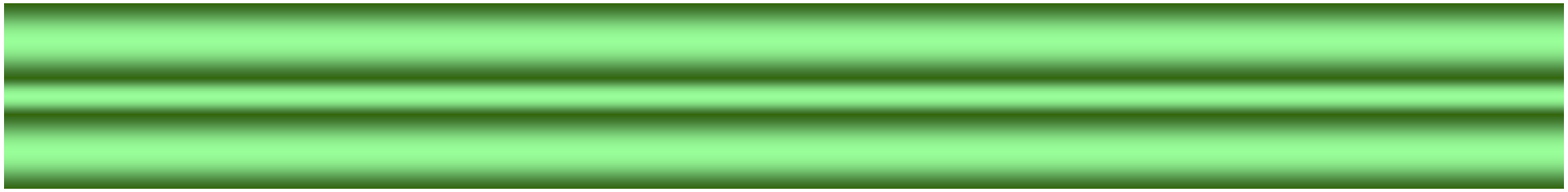
EE414 Embedded Systems

Ch 5. Memory

Part 1/2



Byung Kook Kim
School of Electrical Engineering
Korea Advanced Institute of Science and Technology

Overview

- 5.1 introduction
- 5.2 Memory Write Ability and Storage Performance
- 5.3 Common Memory Types

- 5.4 Composing Memory
- 5.5 Cache
- 5.6 Advanced RAM

5.1 Introduction

- Embedded system's components
  - uP, **mem**, I/O
- Embedded system's functionality aspects
  - Processing
    - processors
    - transformation of data
  - **Storage**
    - Memory ←
    - retention of program & data (for later use)
  - Communication
    - buses
    - transfer of data

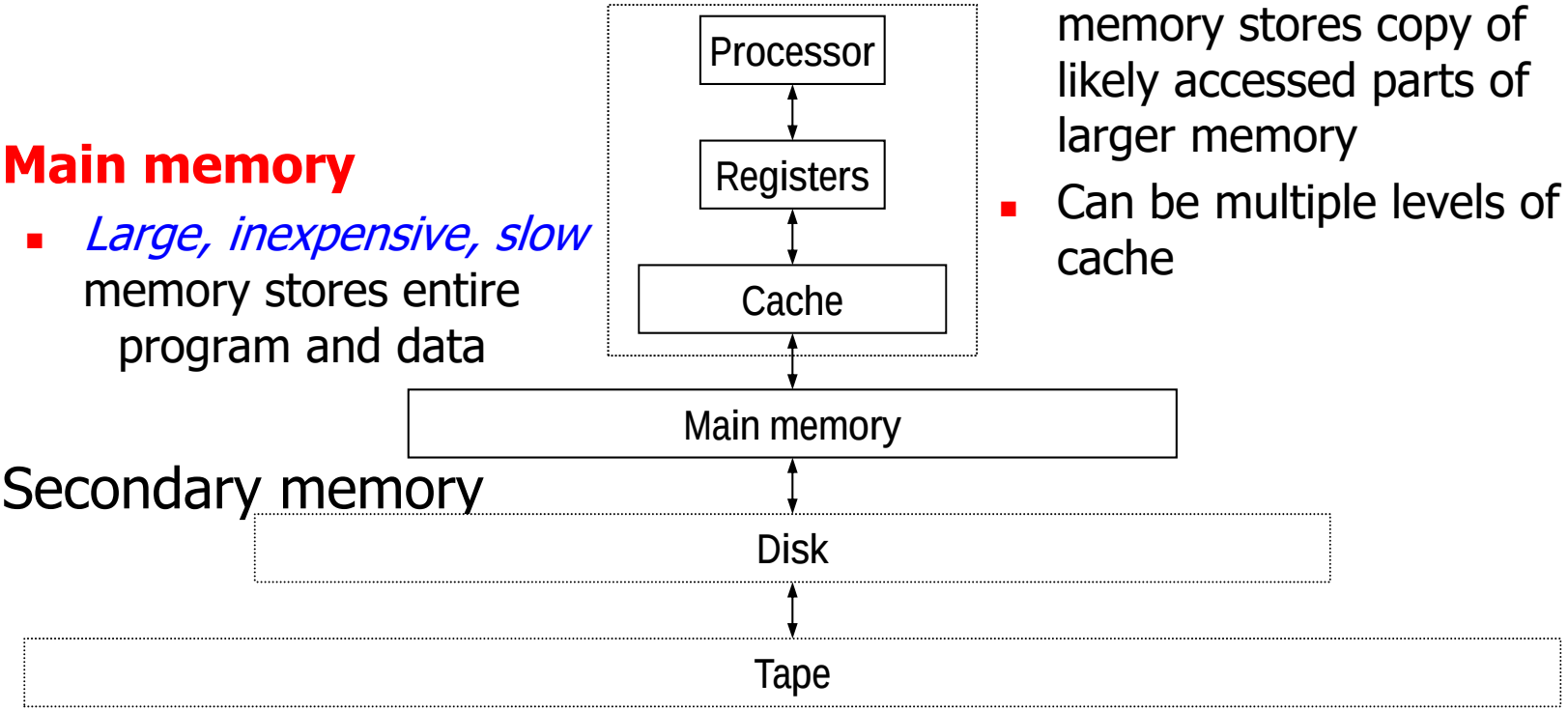
Memory Hierarchy

- Want inexpensive, fast memory

- **Cache**
  - *Small, expensive, fast* memory stores copy of likely accessed parts of larger memory
  - Can be multiple levels of cache

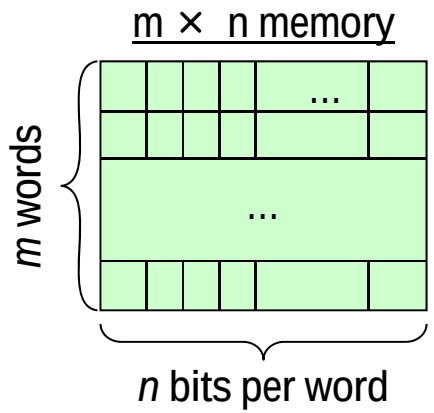
- **Main memory**
  - *Large, inexpensive, slow* memory stores entire program and data

- Secondary memory

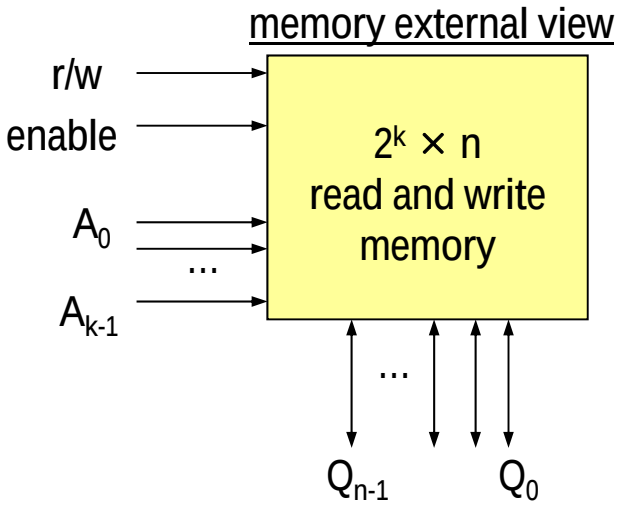


Memory: Basic Concepts

- Stores large number of bits
  - *m* x *n*: *m* words of *n* bits each →
  - Total m*n bits
  - k = $\text{Log}_2(m)$ address input signals
  - or *m* = 2^k words
  - e.g., 4,096 x 8 memory:
    - 32,768 bits
    - 12 address input signals
    - 8 input/output data signals

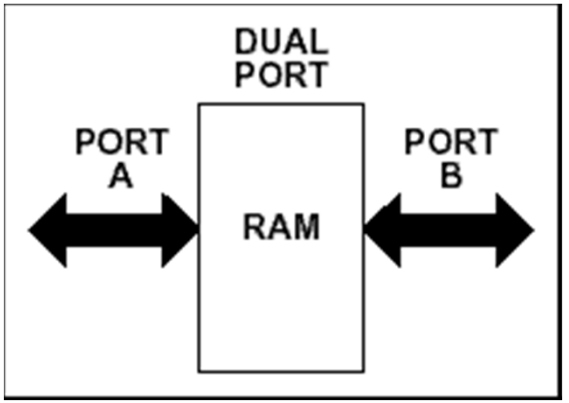


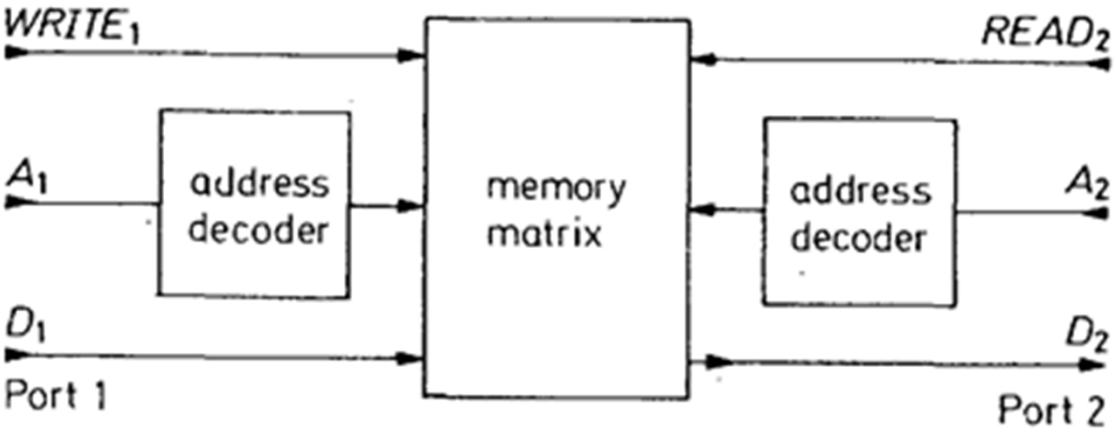
- Memory access (Read or write) →
  - Bus: Data, Address, Control
  - Control signals
    - Enable': read or write only when asserted.
    - r/w': selects read (1) or write (0).



Multi-Port Memory

- Support multiple accesses to different locations simultaneously
  - Multiple sets of control lines, address lines, and data lines
    - One set = a port
  - Ex. Dual-port memory





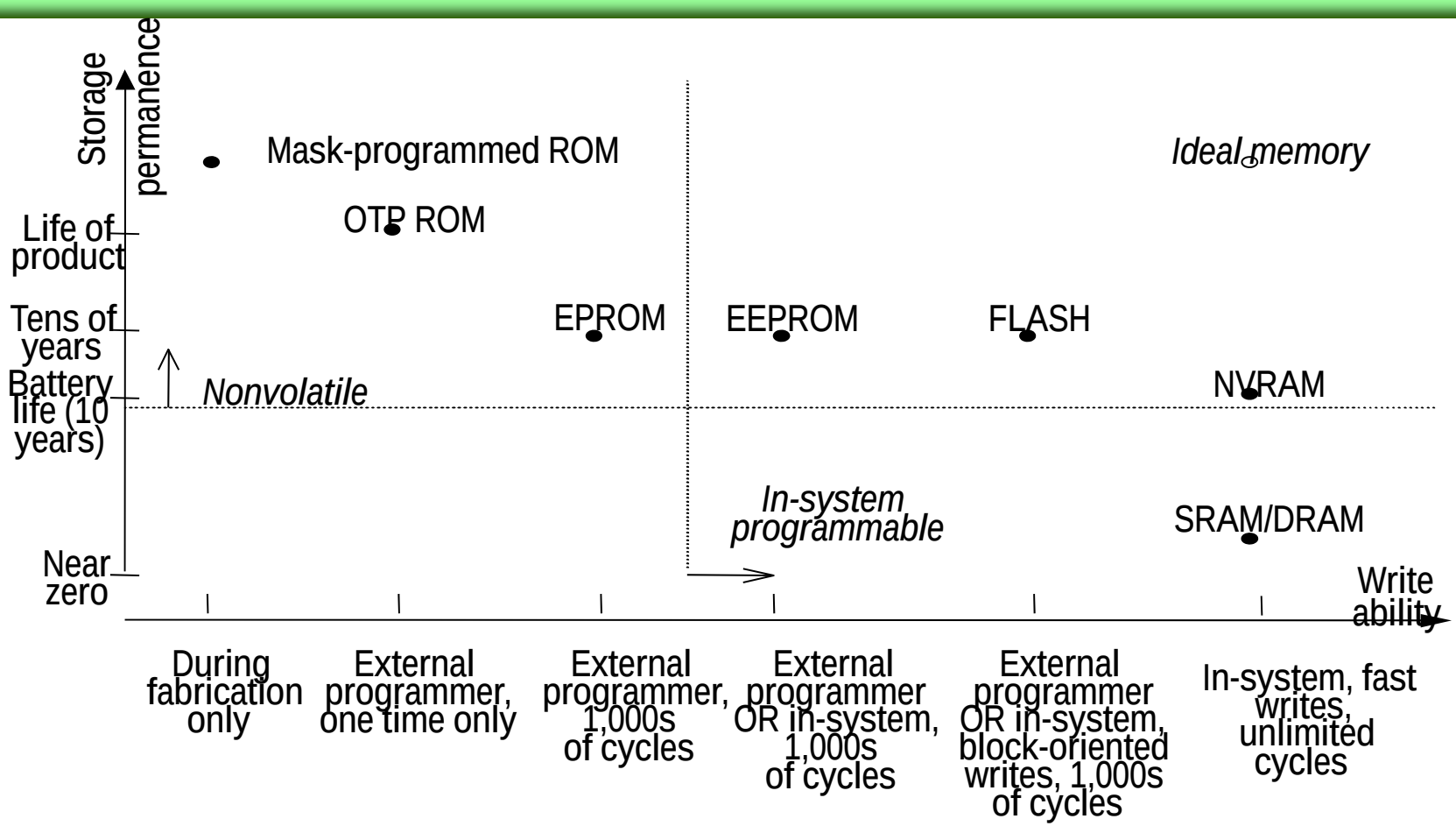
ROM and RAM

- Traditional ROM/RAM distinctions
  - ROM (Read Only Memory)
    - Memory that a processor can only read
    - Retains content when power is off
    - Random Access is possible! ←→ Sequential access
  - RAM (Random Access Memory)
    - Memory that a processor can both read and write
    - Loses its stored bits if power is removed
    - Actually means read write memory!
- Traditional distinctions blurred
  - Advanced ROMs can be written to
    - e.g., EEPROM (Electrically Erasable Programmable ROM)
  - Advanced RAMs can hold bits without power
    - e.g., NVRAM (Non-Volatile RAM)
  - *Distinguish with memory write ability and storage permanence…*

5.2 Memory Write Ability and Storage Permanence

- A. Write ability
  - Manner and speed that a particular memory can be written.
- B. Storage permanence
  - Ability of memory to hold stored bits after they are written.
- Trade offs
  - Write ability and storage permanence tend to be *inversely proportional* to one another.
  - Highly writeable memory typically requires *more area and/or power* than less-writable memory.

Write Ability/ Storage Permanence



Write ability and storage permanence of memories, showing relative degrees along each axis (not to scale).

A. Write Ability

- **Ranges of write ability**
  - High end
    - processor writes to memory simply and quickly: RAM
  - Middle range
    - processor writes to memory, but slower: FLASH, EEPROM
  - Lower range
    - special equipment, "programmer", must be used to write to memory: EPROM, OTP ROM
  - Low end
    - bits stored only during fabrication: Mask-programmed ROM

- In-system programmable memory
  - Can be written to by a processor in the embedded system using the memory ("programming" or "burning")
  - Memories in high end and middle range of write ability

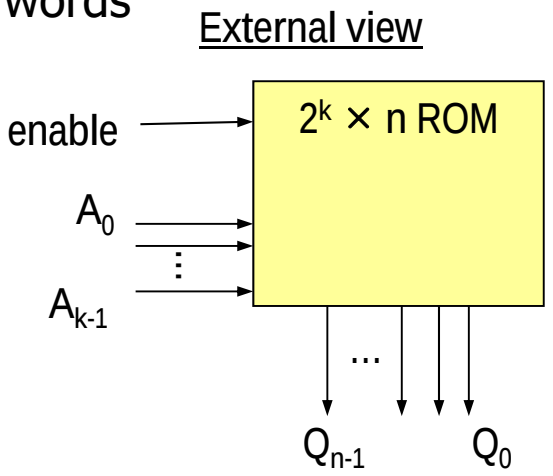
B. Storage Permanence

- **Range of storage permanence**
  - High end
    - essentially never loses bits: Mask-programmed ROM
  - Middle range
    - holds bits years after memory's power source turned off: NVRAM
  - Lower range
    - holds bits as long as power supplied to memory: SRAM
  - Low end
    - begins to lose bits almost immediately after written: DRAM. Refresh required.

- Nonvolatile memory
  - Holds bits after power is no longer supplied
  - High end and middle range of storage permanence

5.3 Common Memory Types
Part 1. ROM: "Read-Only" Memory

- Nonvolatile memory
- Can be read from but not written to, by a processor in an embedded system
- Traditionally written to, "programmed", before inserting to embedded system
- Usages
  - 1) Store software program for general-purpose processor
    - program instructions can be one or more ROM words
  - 2) Store constant data needed by system
  - 3) Implement combinational circuit?!



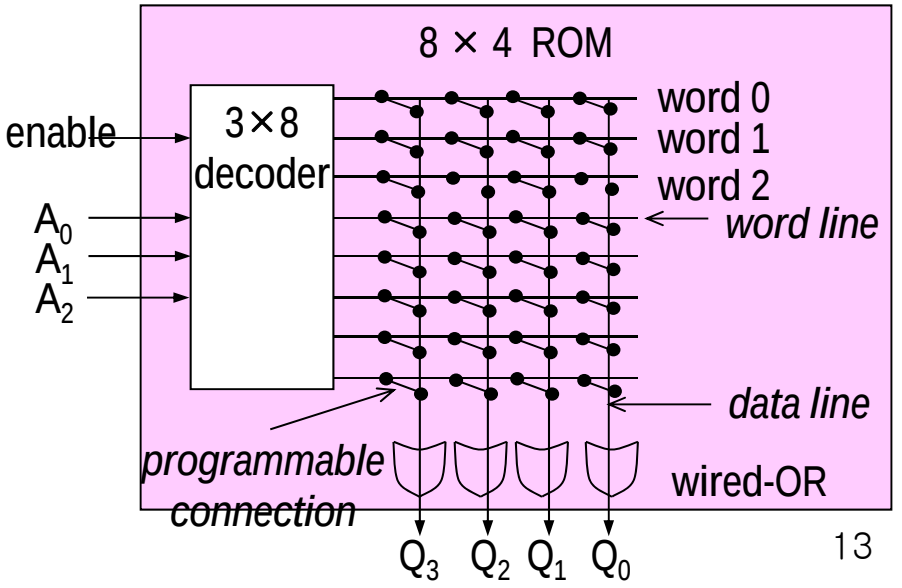
1, 2) Example: 8 x 4 ROM

- Horizontal lines = words
- Vertical lines = data
- Lines connected only at circles (at Fabrication/Lab)

- Address Decoder sets word 2's line to 1 if address input is 010
- Data lines Q_3 and Q_1 are set to 1 because there is a "programmed" connection with word 2's line
- Word 2 is not connected with data lines Q_2 and Q_0

- Data output is 1010!

Internal view

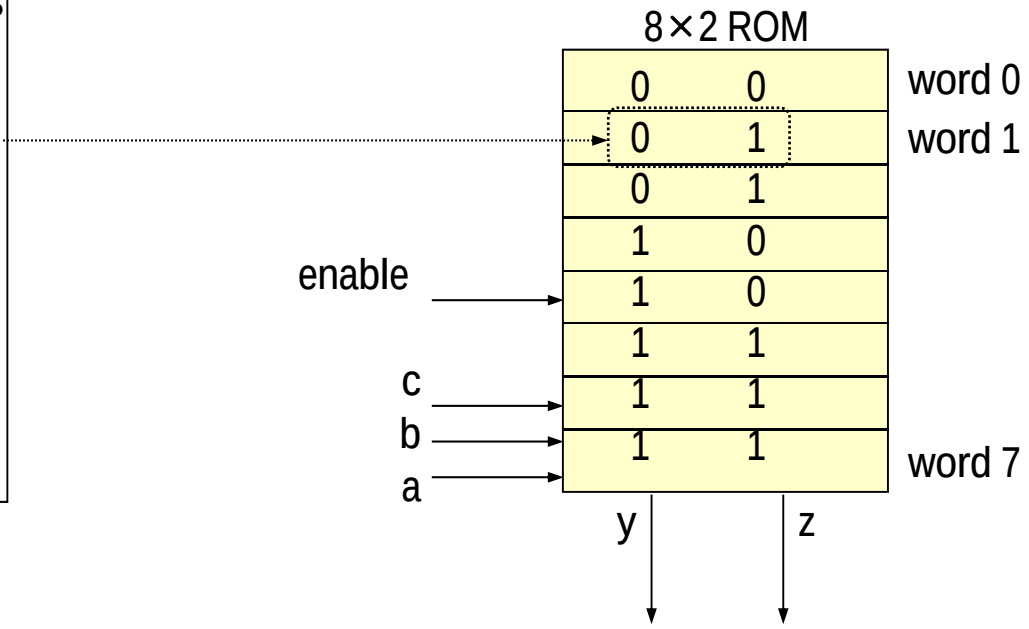


3) Implementing combinational function with ROM

- Any combinational circuit of *n* functions of same *k* variables can be done with 2^*k* x *n* ROM.

Truth table

Inputs (address)			Outputs	
a	b	c	y	z
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

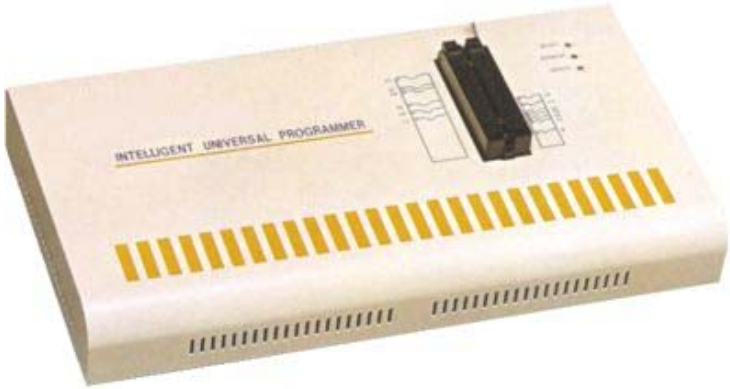


A. Mask-Programmed ROM

- Connections "programmed" at chip fabrication
  - By creating a set of appropriate masks
- Lowest write ability
  - only once!
- Highest storage permanence
  - bits never change unless damaged
- Typically used for final design of high-volume systems
  - spread out NRE cost for a low unit cost

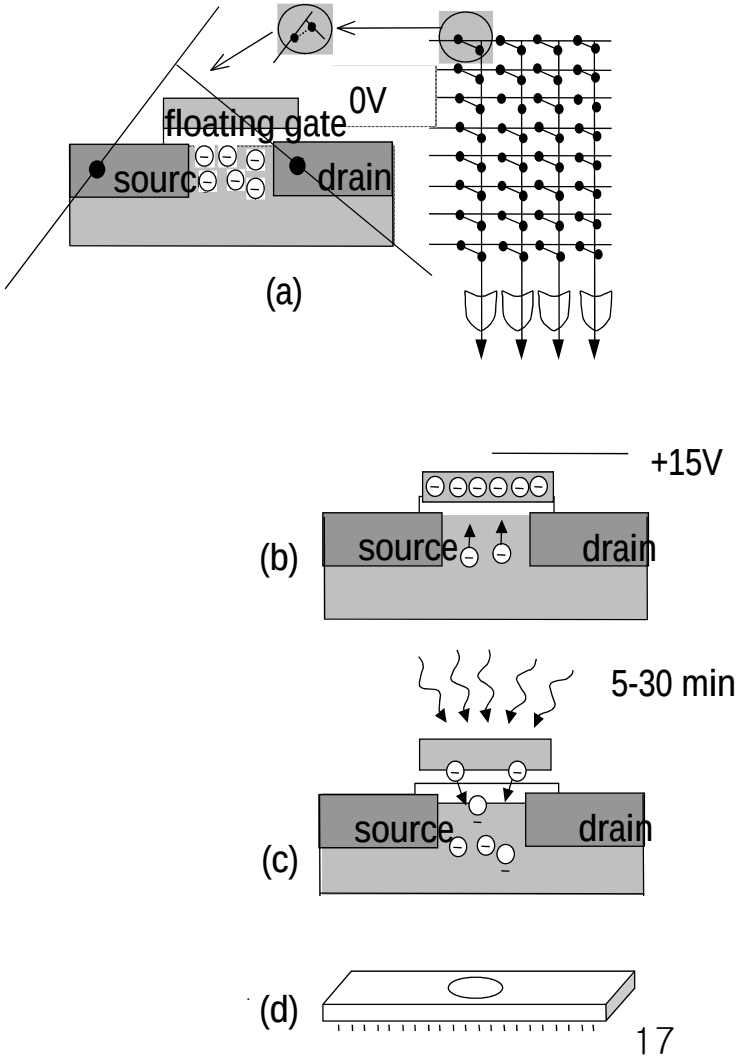
B. OTP ROM: One-Time Programmable ROM

- Connections "programmed" after manufacture by user
  - user provides file of desired contents of ROM
  - file input to machine called *ROM programmer* →
  - each programmable connection is a *fuse*
  - ROM programmer blows fuses with large current where connections should not exist
- Lowest write ability
  - typically written only once and requires ROM programmer device
- Very high storage permanence
  - bits don't change unless reconnected to programmer and more fuses blown
- Commonly used in final products
  - Cheaper.
  - Harder to inadvertently modify.

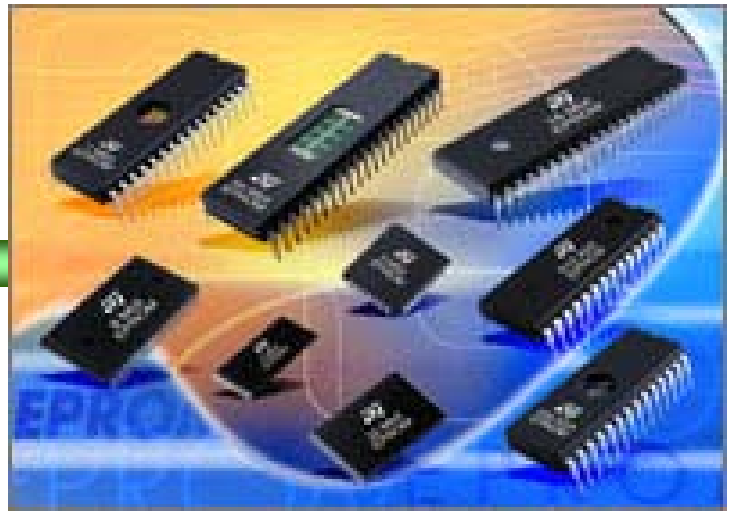


C. EPROM: Erasable Programmable ROM

- **Programmable component is a MOS transistor**
  - Transistor has "floating gate" surrounded by an insulator
  - **(a)** Negative charges form a channel between source and drain storing a logic 1
  - **(b)** Large positive voltage at gate causes negative charges to move out of channel and get trapped in floating gate storing a logic 0 (12 to 25 V)
  - **(c)** (Whole Erase) Shining UV rays on surface of floating-gate causes negative charges to return to channel from floating gate restoring the logic 1 (5 – 30 min)
  - **(d)** An EPROM package showing quartz window through which UV light can pass



EPROM (II)



- Better write ability
  - can be erased and reprogrammed *thousands of times*
- Reduced storage permanence
  - program lasts about *10 years* but is susceptible to radiation and electric noise
  - *A sticker*
- Typically used during design development.

D. EEPROM: Electrically Erasable Programmable ROM

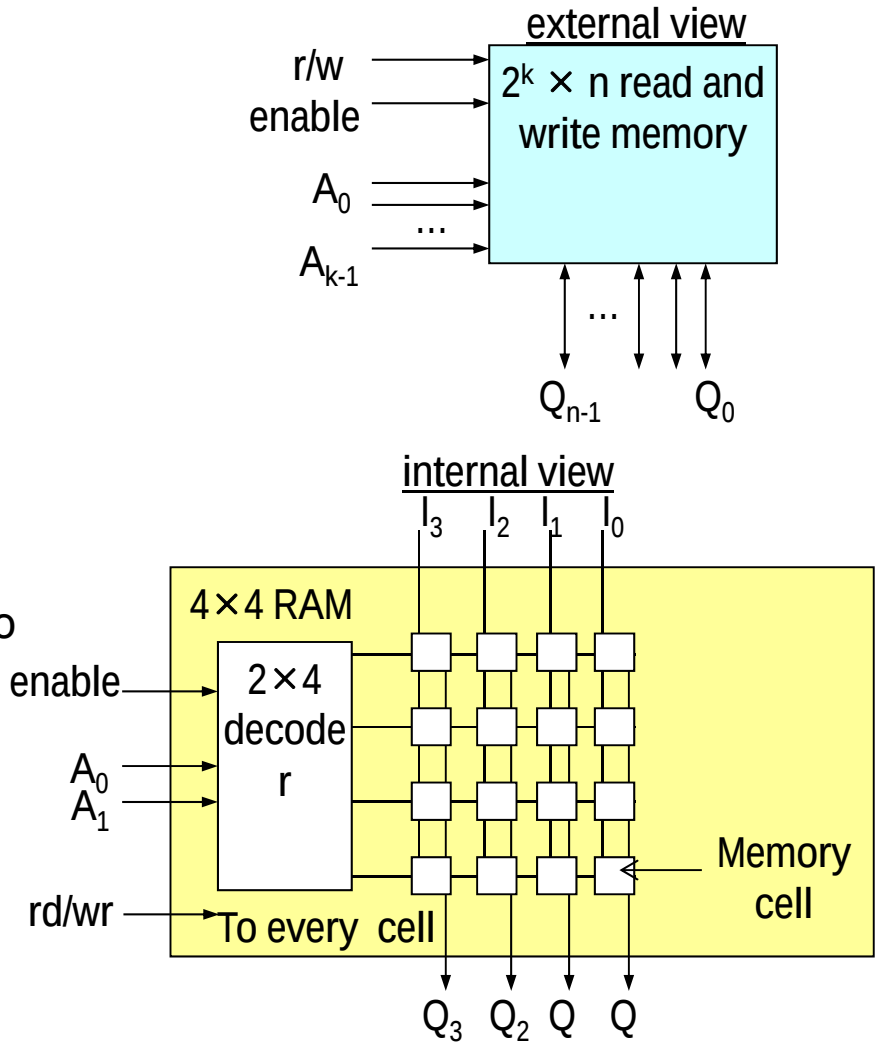
- Programmed and erased electronically (1980's)
  - typically by using *higher than normal voltage in seconds.*
  - can program and erase individual words
- Better write ability
  - can be *in-system programmable* with built-in circuit to provide higher than normal voltage
    - built-in memory controller commonly used to hide details from memory user
  - *writes very slow* (~10 us) due to erasing and programming
    - "busy" pin indicates to processor EEPROM still writing
  - can be erased and programmed *tens of thousands of times*
- Similar storage permanence to EPROM (*about 10 years*)
- Far more convenient than EPROMs, but more expensive.

E. Flash Memory

- Extension of EEPROM (late 1980's)
  - Same floating gate principle
  - Same write ability and storage permanence
- Fast erase
  - Large blocks of memory erased at once, rather than one word at a time
  - Blocks typically several thousand bytes large
- *Cons: Writes to single words may be slower*
  - Entire block must be read, word updated, then entire block written back
- Used with embedded systems storing large data items in nonvolatile memory
  - e.g., digital cameras, TV set-top boxes, cell phones

Part 2. RAM: "Random-Access" Memory

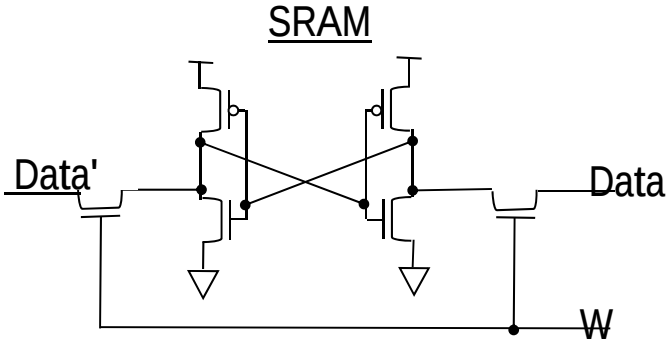
- **Read Write Memory**
- **Typically volatile memory**
  - bits are not held without power supply
- **Read and written to easily by embedded system during execution**
- **Internal structure more complex than ROM**
  - a word consists of several memory cells, each storing 1 bit
  - each input and output data line connects to each cell in its column
  - rd/wr' connected to every cell
  - when row is enabled by decoder, each cell has logic that stores input data bit when rd/wr' indicates write or
  - outputs stored bit when rd/wr' indicates read

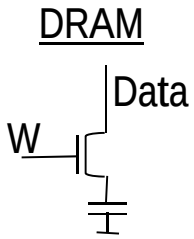


Basic Types of RAM

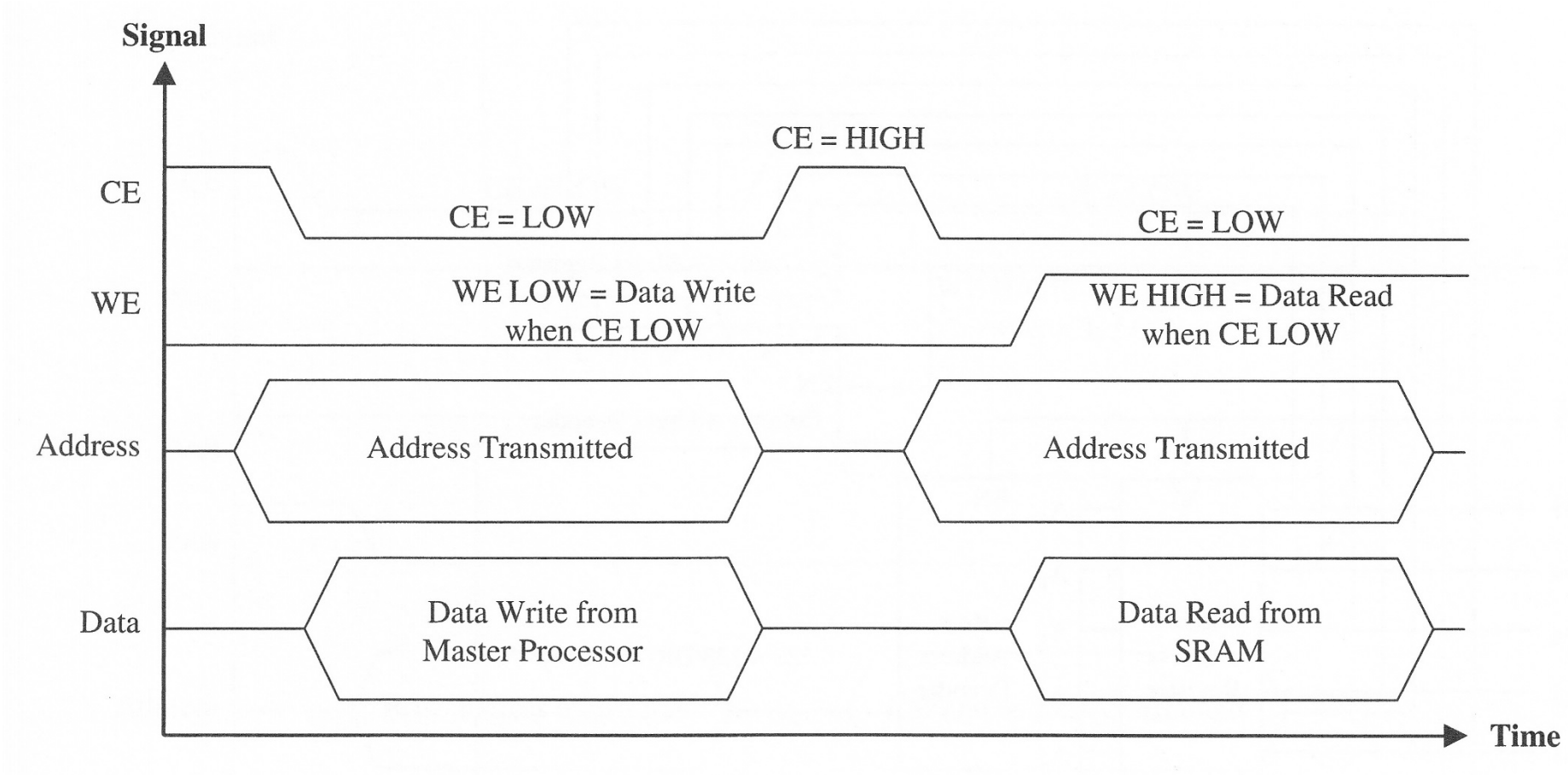
- A. SRAM: Static RAM
  - Memory cell uses flip-flop to store bit
  - Requires 6 transistors/bit
  - Holds data as long as power supplied
- B. DRAM: Dynamic RAM
  - Memory cell uses MOS transistor and capacitor to store bit
  - More compact than SRAM
  - "Refresh" required due to capacitor leak
    - word's cells refreshed when read
  - Typical refresh rate 15.625 microsec.
  - Slower to access than SRAM

memory cell internals





SRAM Timing Diagram

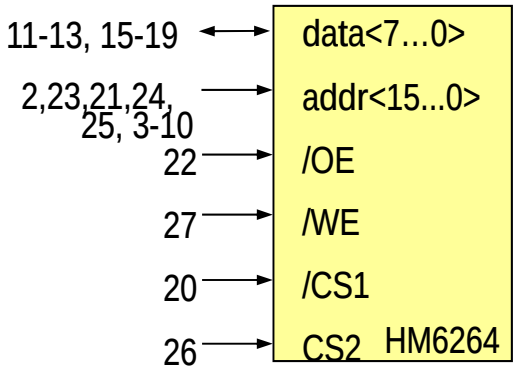


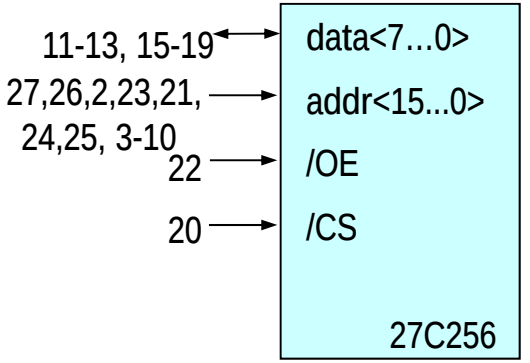
RAM Variations

- C. PSRAM: Pseudo-static RAM
  - DRAM with built-in memory refresh controller
  - Popular low-cost high-density alternative to SRAM
- D. NVRAM: Nonvolatile RAM
  - Holds data after external power removed
  - Battery-backed RAM
    - SRAM with own permanently connected battery (10 years)
    - writes as fast as reads
    - no limit on number of writes unlike nonvolatile ROM-based memory
  - SRAM with EEPROM or Flash
    - stores complete RAM contents on EEPROM or flash before power turned off.

Example: HM6264 & 27C256 RAM/ROM Devices

- Low-cost low-capacity memory devices
- Commonly used in 8-bit microcontroller-based embedded systems
- First two numeric digits indicate device type
  - RAM: 62xxx
  - ROM: 27xxx
- Subsequent digits indicate capacity in kilobits
  - xx64: 64 Kb = 8 KB

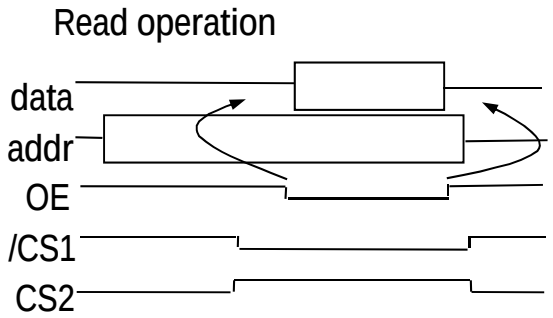


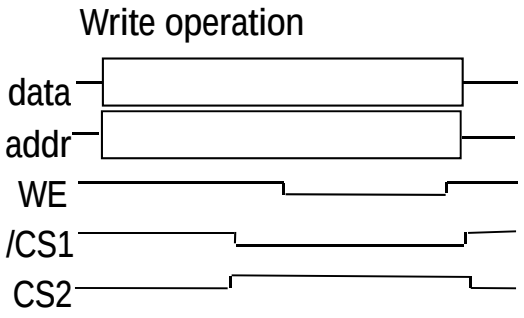


block diagrams

Device	Access Time (ns)	Standby Pwr. (mW)	Active Pwr. (mW)	Vcc Voltage (V)
HM6264	85-100	.01	15	5
27C256	90	.5	100	5

device characteristics

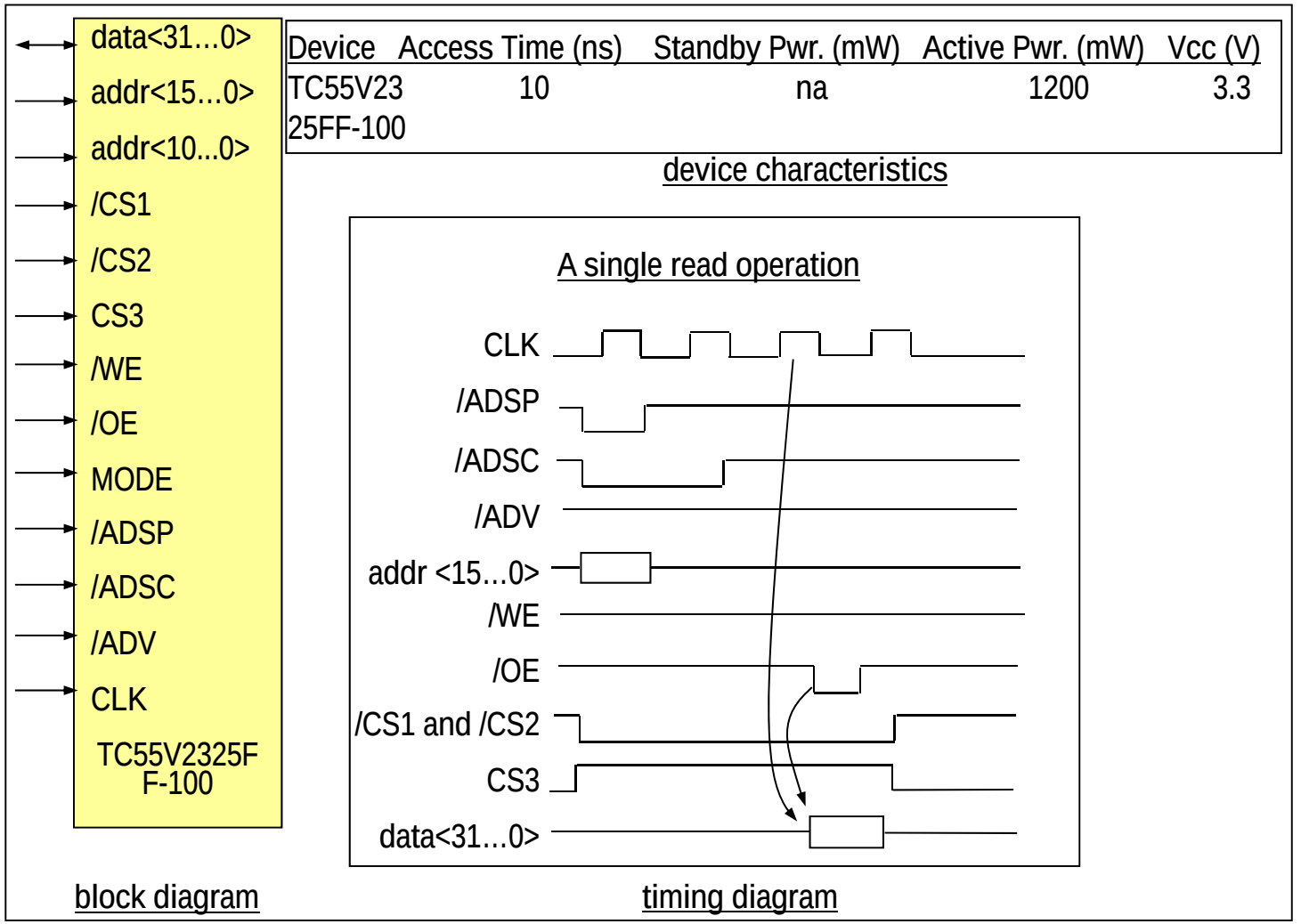




timing diagrams

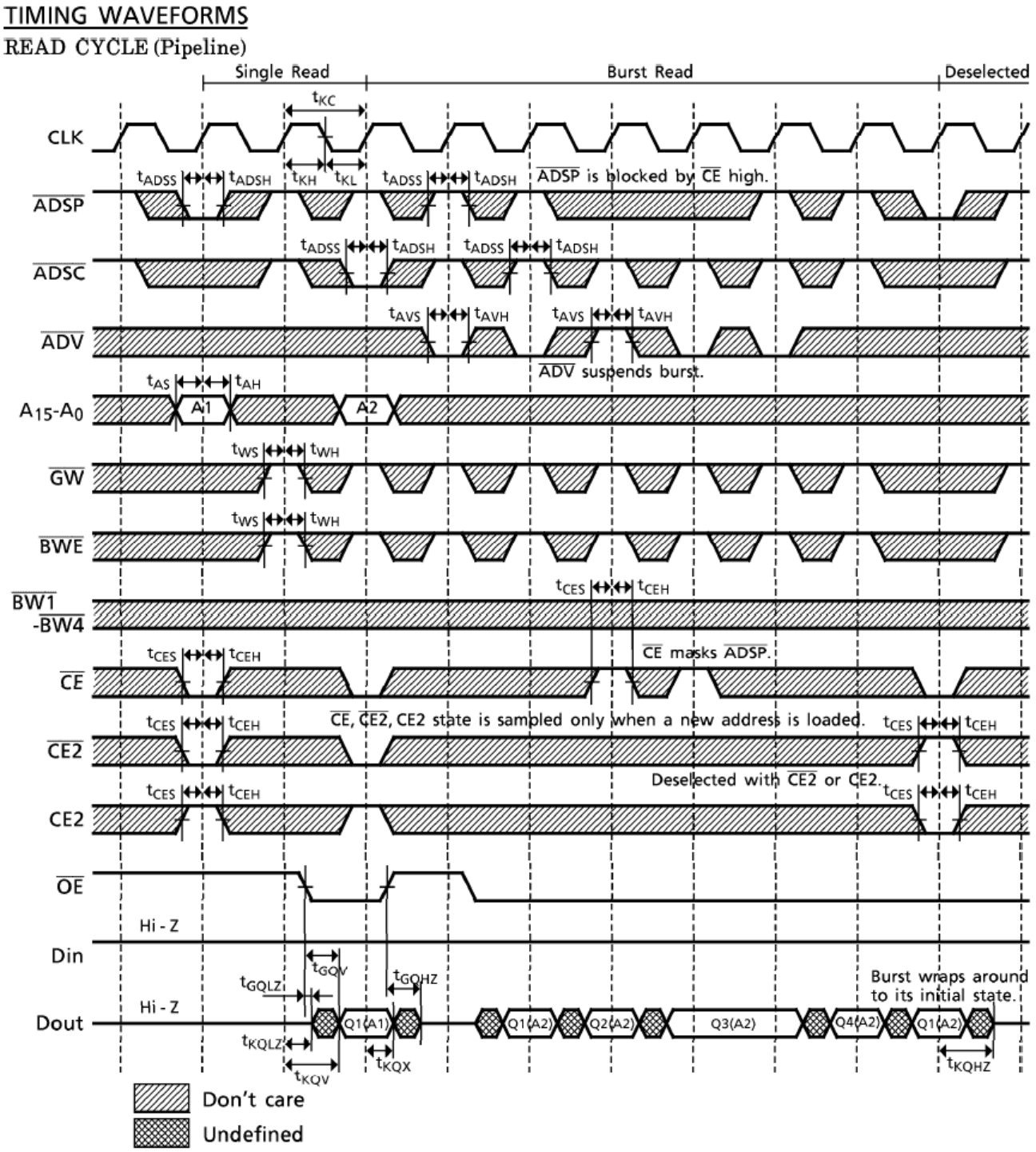
Example: TC55V2325FF-100 memory device

- 2-megabit synchronous pipelined burst SRAM memory device
- Designed to be interfaced with 32-bit processors
- Capable of fast sequential reads and writes.



TC55V232FF

- Read pipeline
  - ADV' (Address Advance) low
  - Keep incrementing address register.



References

- [1] Frank Vahid, “Embedded system design: A unified hardware/software introduction”, John Wiley & Sons, 2002.